WHAT IS CLAIMED IS:

1. A method for fabricating a BiCMOS integrated circuit, comprising the steps of:

forming in a single implantation step a base region of a bipolar transistor and a p-well of an n-channel MOS transistor; and

forming in a single implantation step a collector contact well of a bipolar transistor and an n-well of a p-channel MOS transistor.

2. A method for fabricating a BiCMOS integrated circuit, comprising the steps of:

forming an n-type collector region within a semiconductor substrate of lighter doping;

forming a plurality of p-type wells, at least one of said plurality of p-type wells forming a base region lying between said collector region and a surface of said semiconductor substrate, said base region adjoining said collector region and extending to said surface, and at least one of said plurality of p-type wells forming an n-channel MOS well;

forming a plurality of n-type wells, at least one of said plurality of n-type wells forming a collector contact well lying between said collector region and said surface of said semiconductor substrate, said collector contact well adjoining said collector region and extending to said surface, further said collector contact well lying between said base region and said n-channel MOS well, and at least one of said plurality of n-type wells forming a p-channel MOS well; and

forming an emitter region adjoining said base region, said emitter region extending to said surface.

3. The method of Claim 2, further including the step of implanting p-dopants into said p-type wells, excluding a portion of said base region adjacent said emitter region.

4. The method of Claim 3, further including the step of implanting n-type dopants into said n-type wells and into a portion of said base region.

5. The method of Claim 2, further including the step of implanting n-type dopants into said n-type wells and into a portion of said base region.

6. A bipolar transistor, comprising:

a collector region of a first doping profile within a semiconductor substrate of lighter doping;

a base region between said collector region and a surface of said semiconductor substrate, said base region adjoining said collector region and extending to said surface;

an emitter region adjoining said base region, said emitter region extending to said surface; and

a well region adjoining said collector region and said base region and extending to said surface, said well region having a doping profile characterized by doping concentrations lighter than doping concentrations of said first doping profile.

7. The transistor of Claim 6, wherein said base region is characterized by a substantially uniform lateral doping profile.

8. The transistor of Claim 6, wherein said base region is characterized by a lighter doping concentration in a region adjacent said emitter region.

9. A BiCMOS integrated circuit, comprising:

(a) a bipolar transistor including a collector well contact region; and

(b) a MOS transistor having source and drain contacts formed in an n-well region, said collector well contact region and said n-well region having substantially the same dopant profile.

10. A BiCMOS integrated circuit, comprising:

(a) a bipolar transistor including:

a collector region within a semiconductor substrate, said collector region having a first dopant profile;

a base region between said collector region and a surface of said semiconductor substrate, said base region adjoining said collector region and extending to said surface, further said base region having a second doping profile;

an emitter region adjoining said base region, said emitter region extending to said surface; and

a collector contact well region adjoining said collector region and said base region and extending to said surface, said collector contact well region having a third doping profile, said third doping profile characterized by lighter doping concentrations than said first doping profile;

(b) an n-channel MOS transistor having source and drain contacts formed in a doped well region having said second doping profile; and

(c) a p-channel MOS transistor having source and drain contacts formed in a well region having said third doping profile.

11. The integrated circuit of Claim 10, wherein said base region comprises a region of lighter dopant concentration adjacent said emitter region.